

Entry  
approved  
HHR  
8/27/02

RESPONSE UNDER 37 CFR 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 2818PATENT APPLICATION  
Do. No. 5038-062

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: John B. Halbert and Randy M. Bonella

Serial No.: 09/666,528

Examiner: Huan Hoang

Filed: September 18, 2000

Group Art Unit: 2818

For: MEMORY SYSTEM HAVING BUFFERS FOR ISOLATING  
STACKED MEMORY DEVICES

Date: August 20, 2002

BOX AF

Assistant Commissioner for Patents  
Washington, DC 20231

11/Suppl.  
Amend  
J. Hoa  
G. Staley  
8-21-02

SUPPLEMENTAL AMENDMENT AFTER  
FINAL REJECTION UNDER 37 CFR 1.116

In response to the Final Office Action dated March 12, 2002 and supplementing the Response to Final Office Action dated July 22, 2002, please amend the application as follows.

IN THE CLAIMS

FAX COPY RECEIVED

Please rewrite claims 20 and 21 as follows:

'AUG 20 2002  
TECHNOLOGY CENTER 2807

13. (Amended) A memory system comprising:

a bus;

a stack of memory devices;

a buffer coupled between the stack of memory devices and the ~~memory~~ bus; and  
a memory controller coupled to the bus.16.  
17. (Amended) A memory system comprising:

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